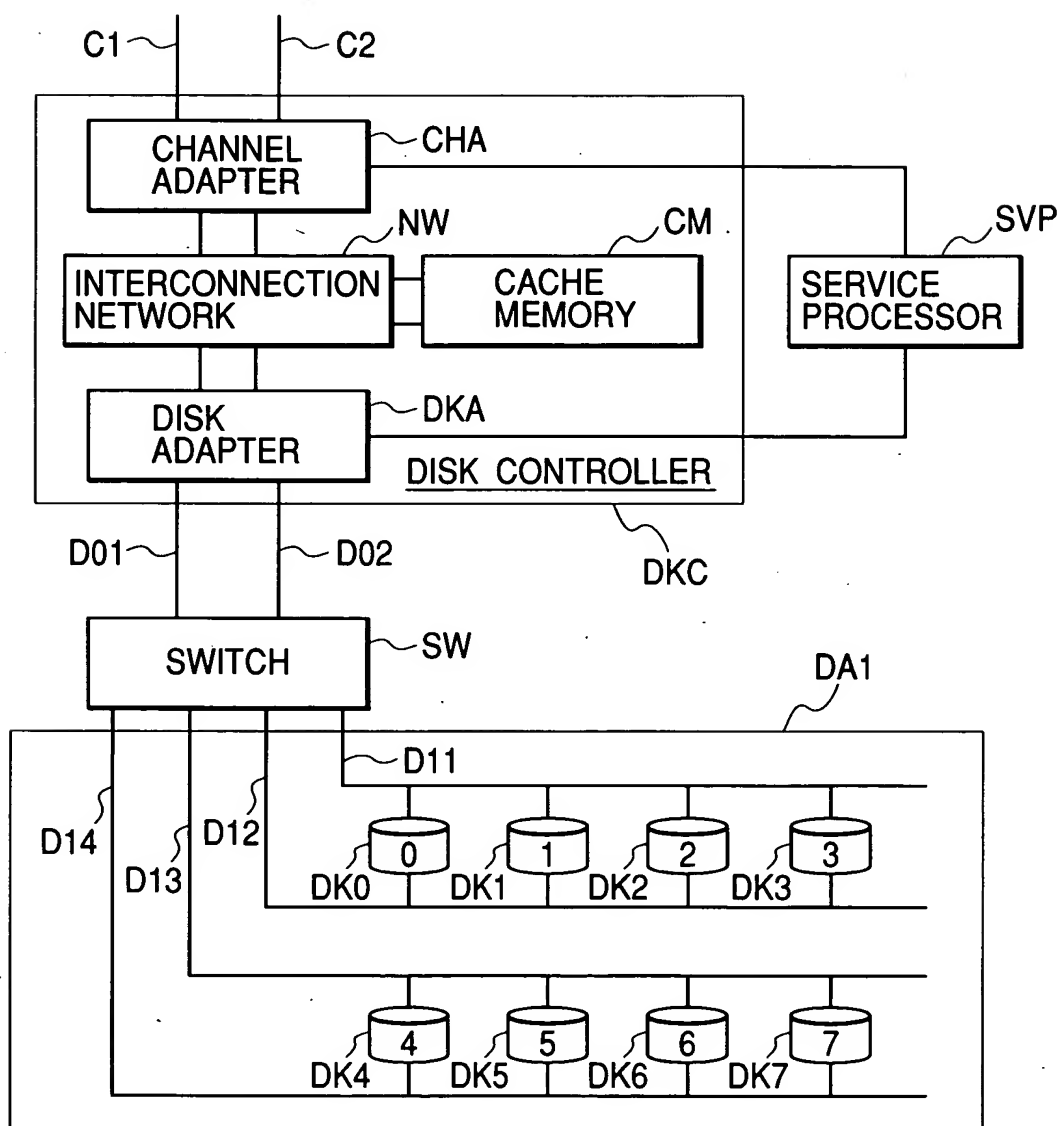
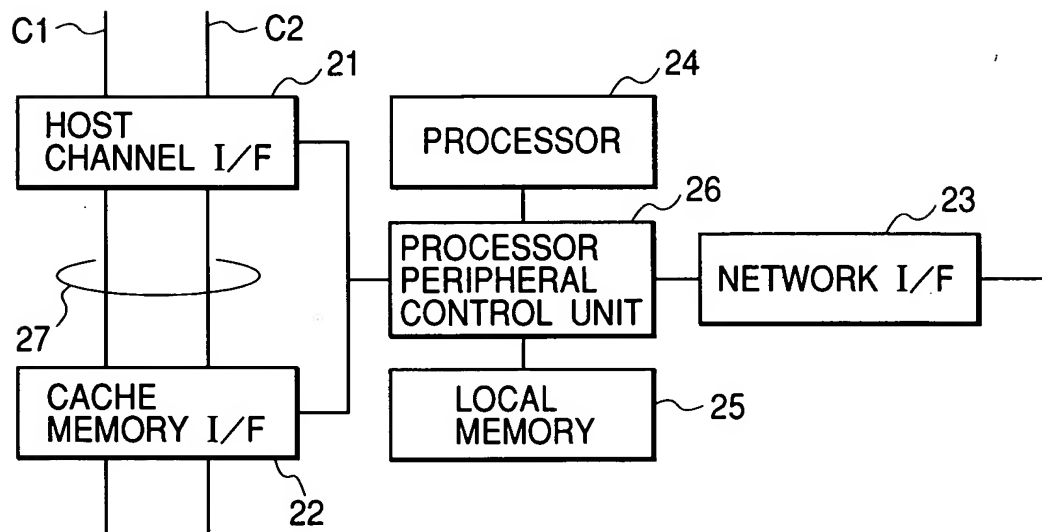
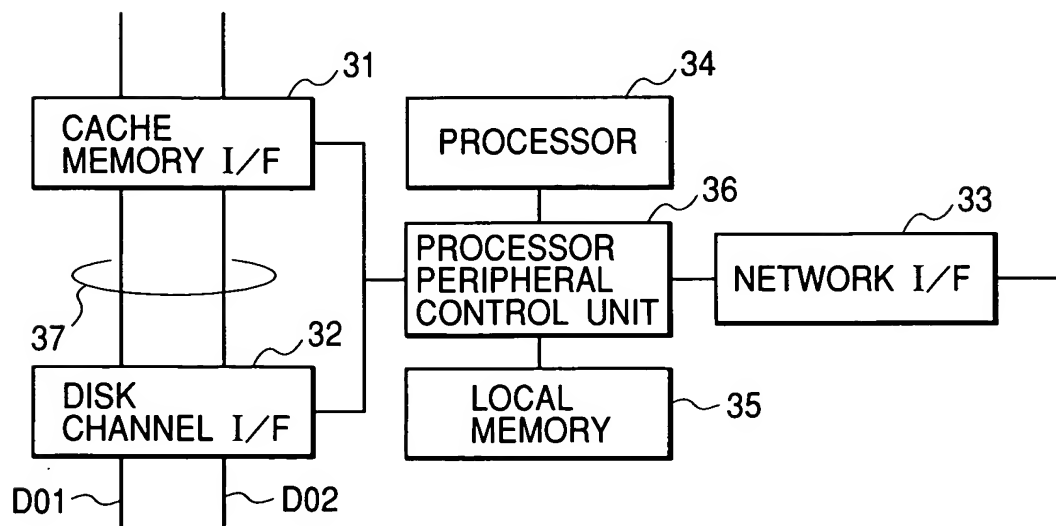


FIG. 1

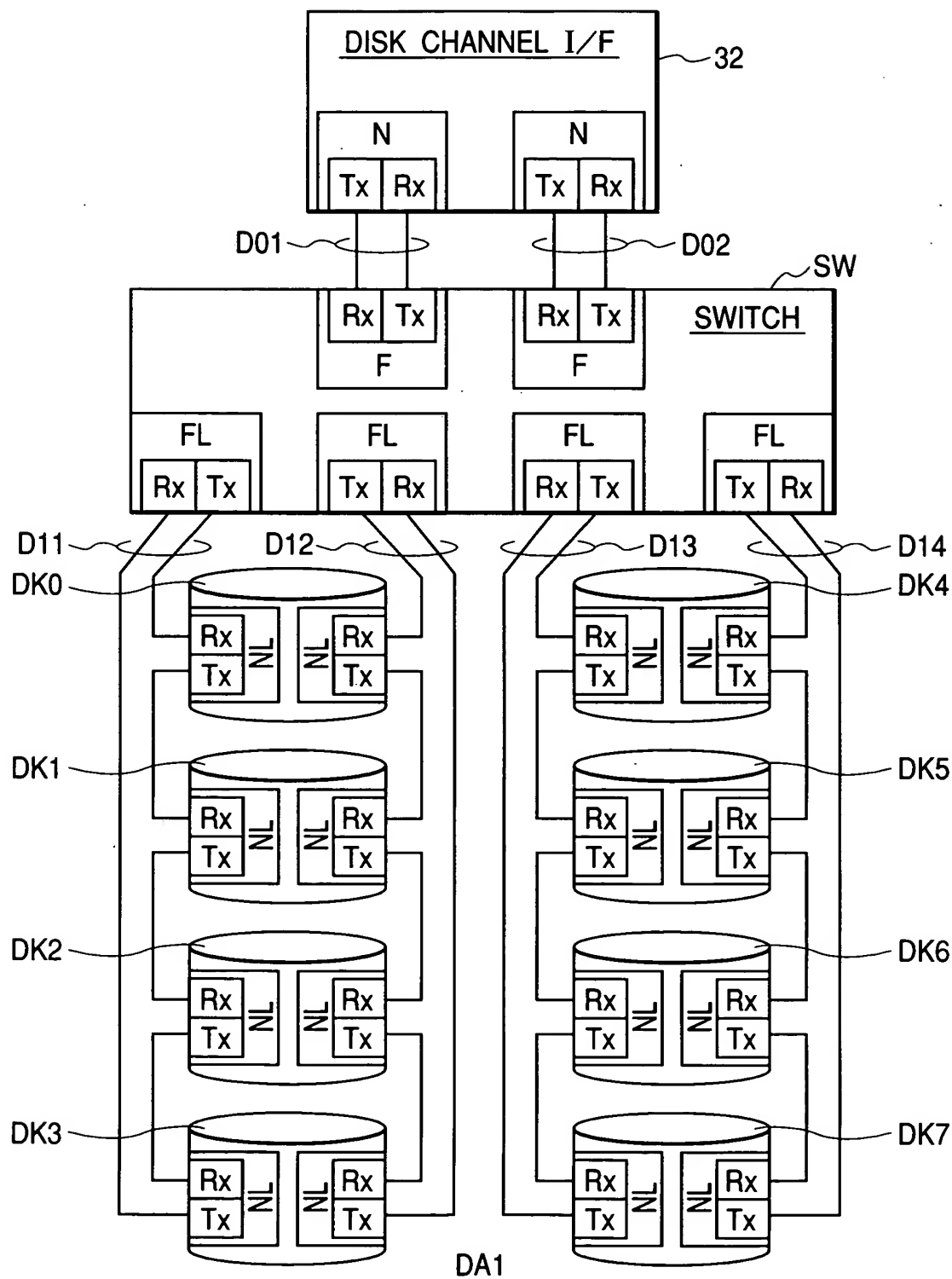


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FIG. 2CONFIGURATION OF CHANNEL ADAPTER CHA**FIG. 3**CONFIGURATION OF DISK ADAPTER DKA

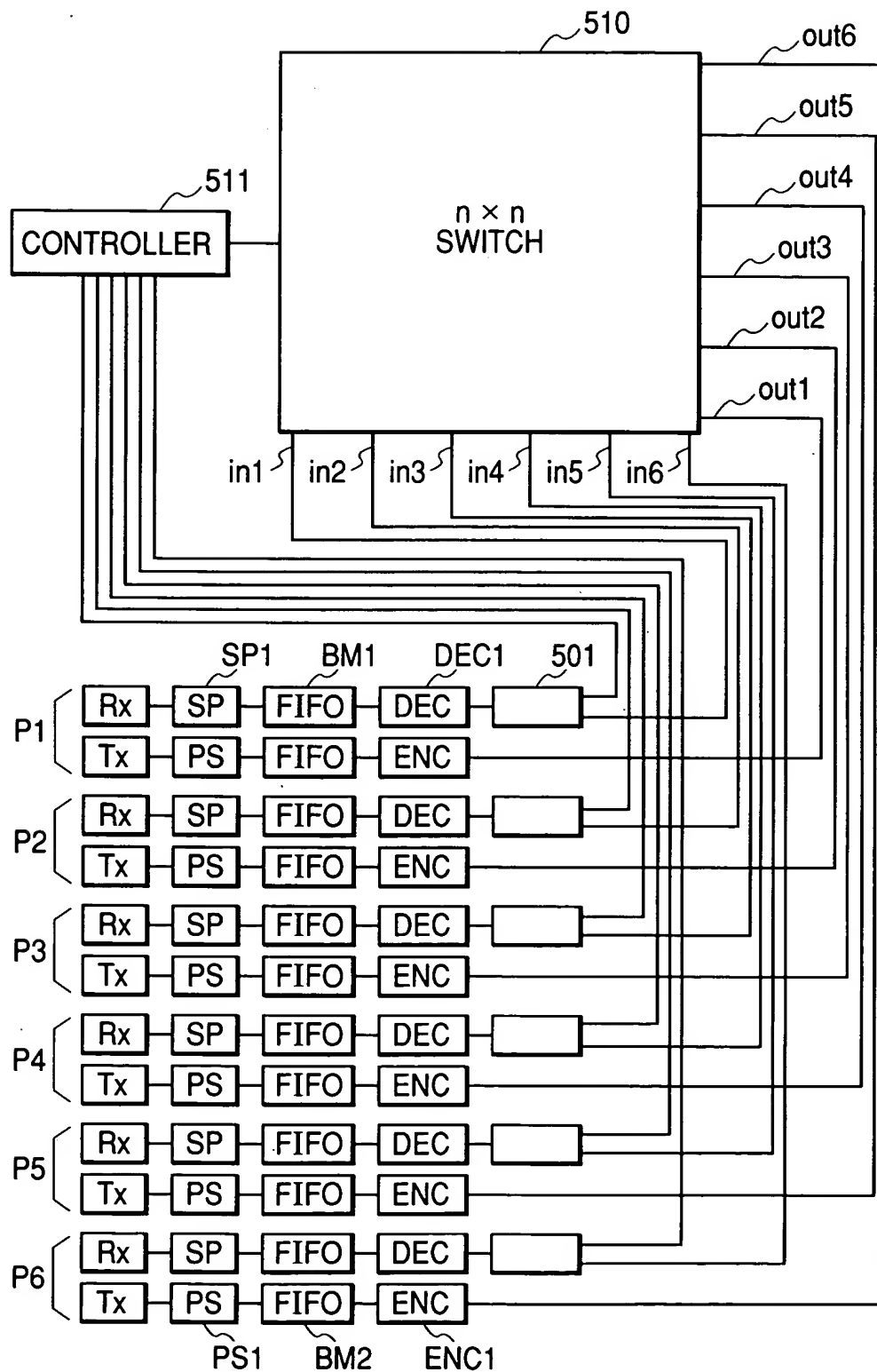
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FIG. 4



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FIG. 5



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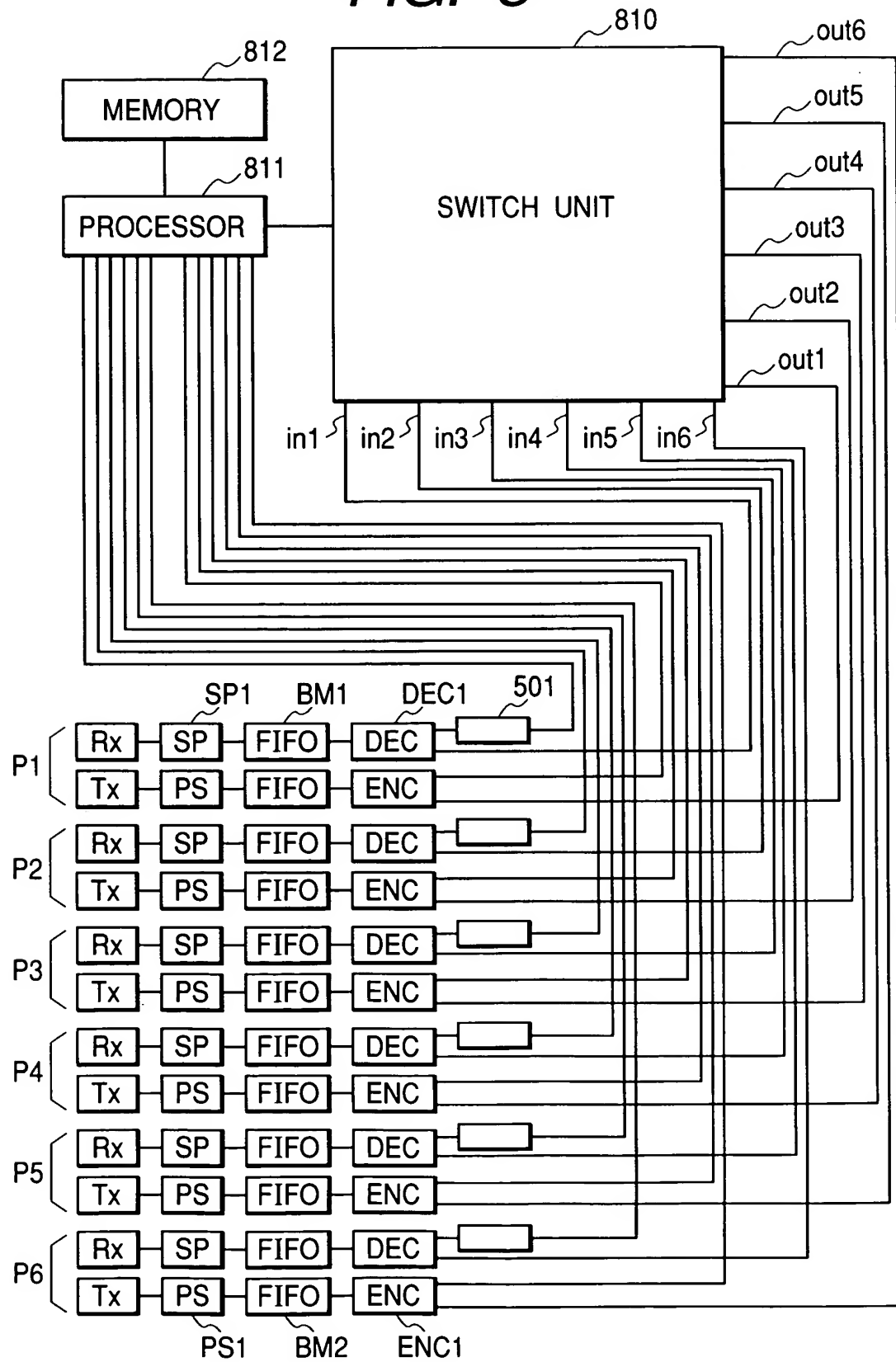
FIG. 6

	601		602		603	
	WITHOUT FAILURE		WHEN PORT "a" FAILS		WHEN PORT "b" FAILS	
DRIVE NO.	Read	Write	Read	Write	Read	Write
0	PID_0. a	PID_0. b	PID_0. b		PID_0. a	
1	PID_1. a	PID_1. b	PID_1. b		PID_1. a	
2	PID_2. a	PID_2. b	PID_2. b		PID_2. a	
3	PID_3. a	PID_3. b	PID_3. b		PID_3. a	
4	PID_4. a	PID_4. b	PID_4. b		PID_4. a	
5	PID_5. a	PID_5. b	PID_5. b		PID_5. a	
6	PID_6. a	PID_6. b	PID_6. b		PID_6. a	
7	PID_7. a	PID_7. b	PID_7. b		PID_7. a	

FIG. 7

	701		WHEN PORT "a" FAILS		WHEN PORT "b" FAILS	
DRIVE NO.	Read	Write	Read	Write	Read	Write
0	PID_0. a	PID_0. b	PID_0. b		PID_0. a	
1	PID_1. b	PID_1. a	PID_1. b		PID_1. a	
2	PID_2. a	PID_2. b	PID_2. b		PID_2. a	
3	PID_3. b	PID_3. a	PID_3. b		PID_3. a	
4	PID_4. a	PID_4. b	PID_4. b		PID_4. a	
5	PID_5. b	PID_5. a	PID_5. b		PID_5. a	
6	PID_6. a	PID_6. b	PID_6. b		PID_6. a	
7	PID_7. b	PID_7. a	PID_7. b		PID_7. a	

FIG. 8



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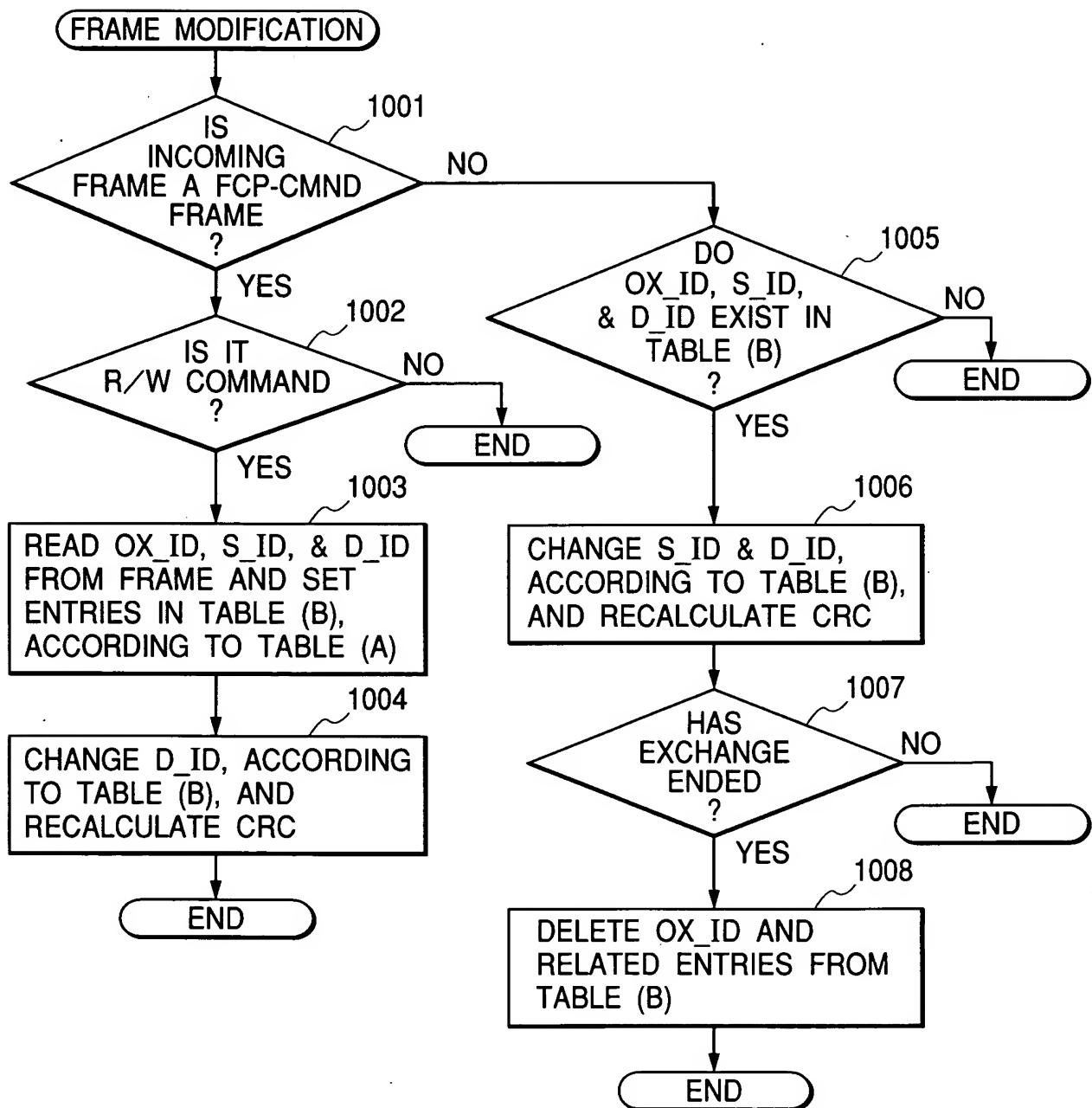
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FIG. 9

Word	SOFi3				
0	R_CTL	D_ID			901
1	CS_CTL	S_IS			902
2	TYPE	F_CTL			906
3	SEQ_ID	DF_CTL	SEQ_CNT		
4	OX_ID		RX_ID		903
5	[00 00 00 00]				
6					
7	LUN				
8	(TASK MANAGEMENT FLAG AND OTHERS)				904
9	CDB Byte0	CDB Byte1	CDB Byte2	CDB Byte3	
10	CDB Byte4	CDB Byte5	CDB Byte6	CDB Byte7	
11	CDB Byte8	CDB Byte9	CDB Byte10	CDB Byte11	
12	CDB Byte12	CDB Byte13	CDB Byte14	CDB Byte15	
13	FCP_DL				
	CRC				
	EOFt				

FIG. 10



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FIG. 11B

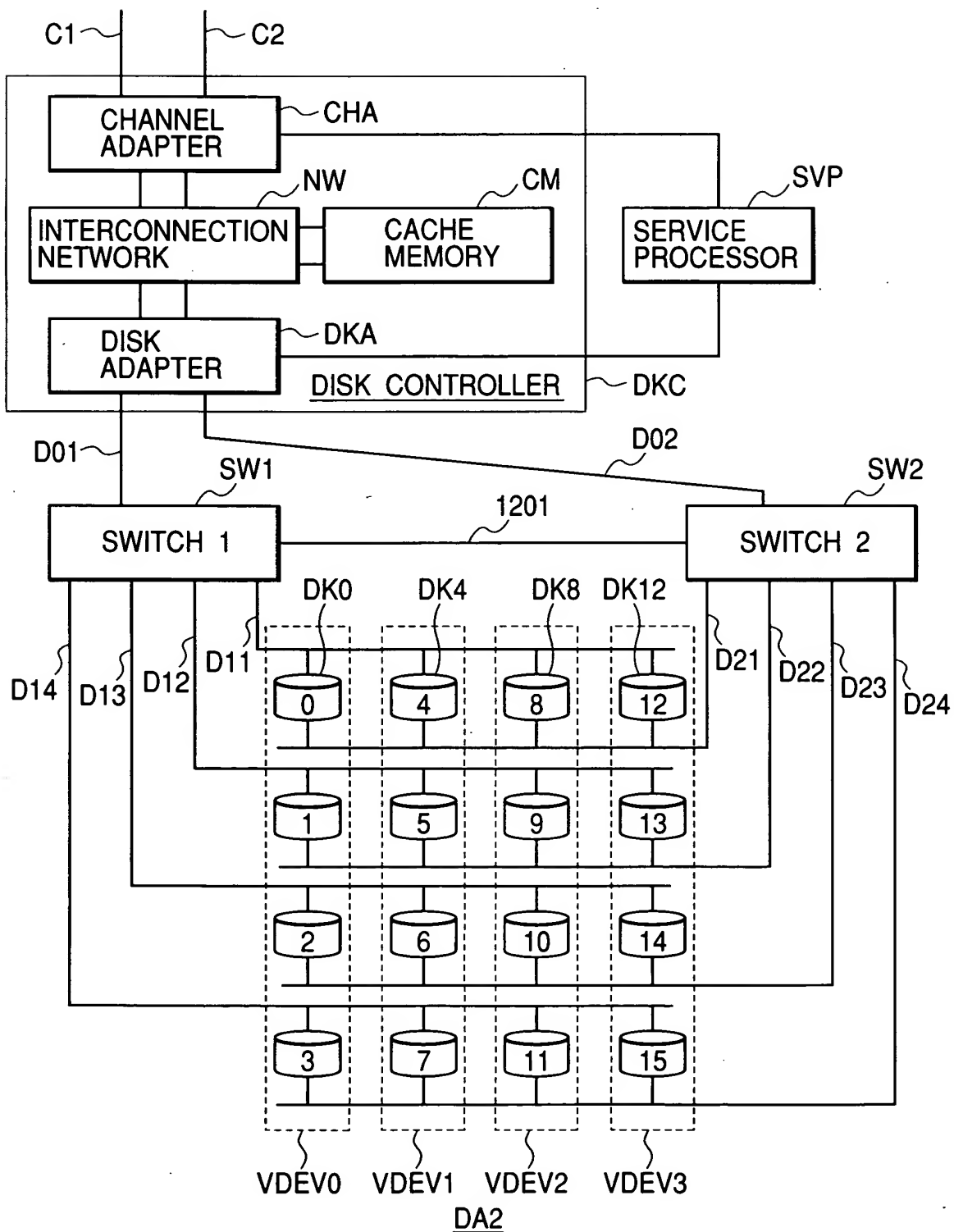
[illegible]

FIG. 11A

Drive Port_ID	Read	Write
PID_0. a	PID_0. a	PID_0. b
PID_0. b	PID_0. a	PID_0. b
PID_1. a	PID_1. a	PID_1. b
PID_1. b	PID_1. a	PID_1. b
PID_2. a	PID_2. a	PID_2. b
PID_2. b	PID_2. a	PID_2. b
PID_3. a	PID_3. a	PID_3. b
PID_3. b	PID_3. a	PID_3. b
PID_4. a	PID_4. a	PID_4. b
PID_4. b	PID_4. a	PID_4. b

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FIG. 12



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FIG. 13

		WITHOUT FAILURE			WHEN SW1 FAILS		WHEN SW2 FAILS	
DRIVE NO.	VDEV	DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R/W Drive Port
0	0	0	PID_0. a	PID_0. b	1	PID_0. b	0	PID_0. a
1			PID_1. a	PID_1. b		PID_1. b		PID_1. a
2			PID_2. a	PID_2. b		PID_2. b		PID_2. a
3			PID_3. a	PID_3. b		PID_3. b		PID_3. a
4	1	0	PID_4. a	PID_4. b	1	PID_4. b	0	PID_4. a
5			PID_5. a	PID_5. b		PID_5. b		PID_5. a
6			PID_6. a	PID_6. b		PID_6. b		PID_6. a
7			PID_7. a	PID_7. b		PID_7. b		PID_7. a
8	2	0	PID_8. a	PID_8. b	1	PID_8. b	0	PID_8. a
9			PID_9. a	PID_9. b		PID_9. b		PID_9. a
10			PID_10. a	PID_10. b		PID_10. b		PID_10. a
11			PID_11. a	PID_11. b		PID_11. b		PID_11. a
12	3	0	PID_12. a	PID_12. b	1	PID_12. b	0	PID_12. a
13			PID_13. a	PID_13. b		PID_13. b		PID_13. a
14			PID_14. a	PID_14. b		PID_14. b		PID_14. a
15			PID_15. a	PID_15. b		PID_15. b		PID_15. a

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FIG. 14A

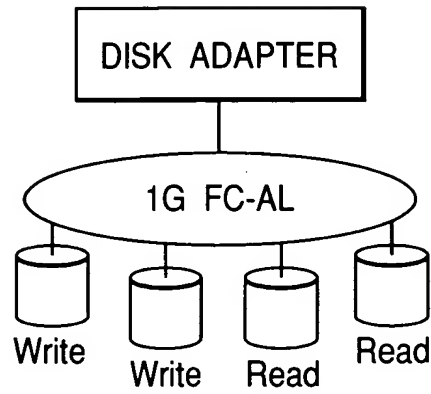


FIG. 14B

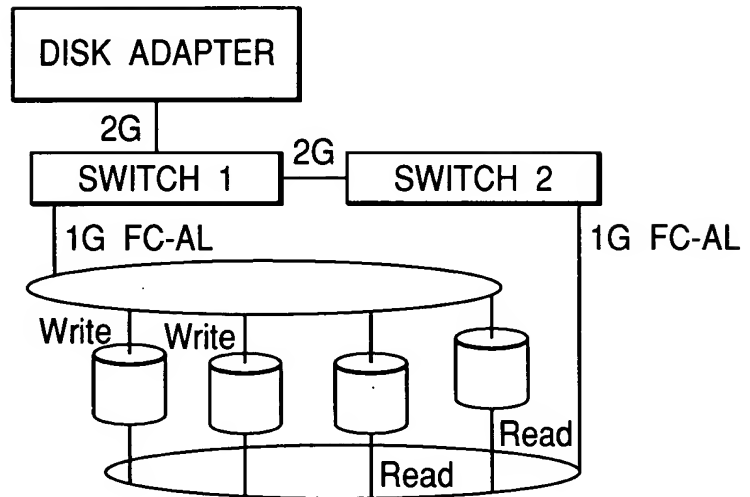
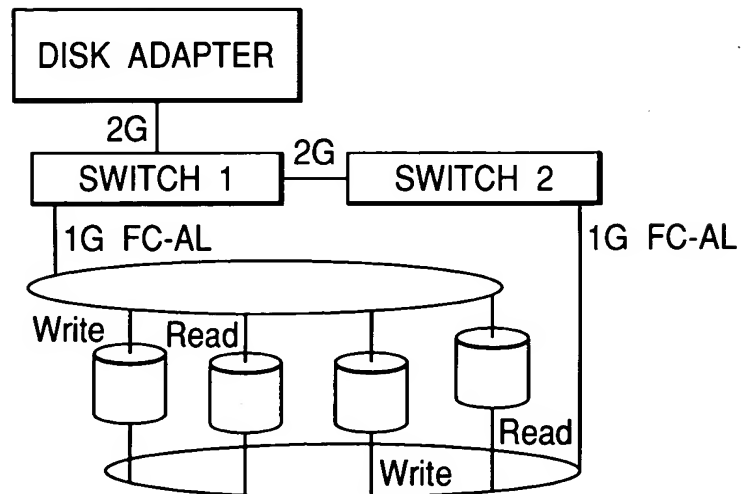


FIG. 14C



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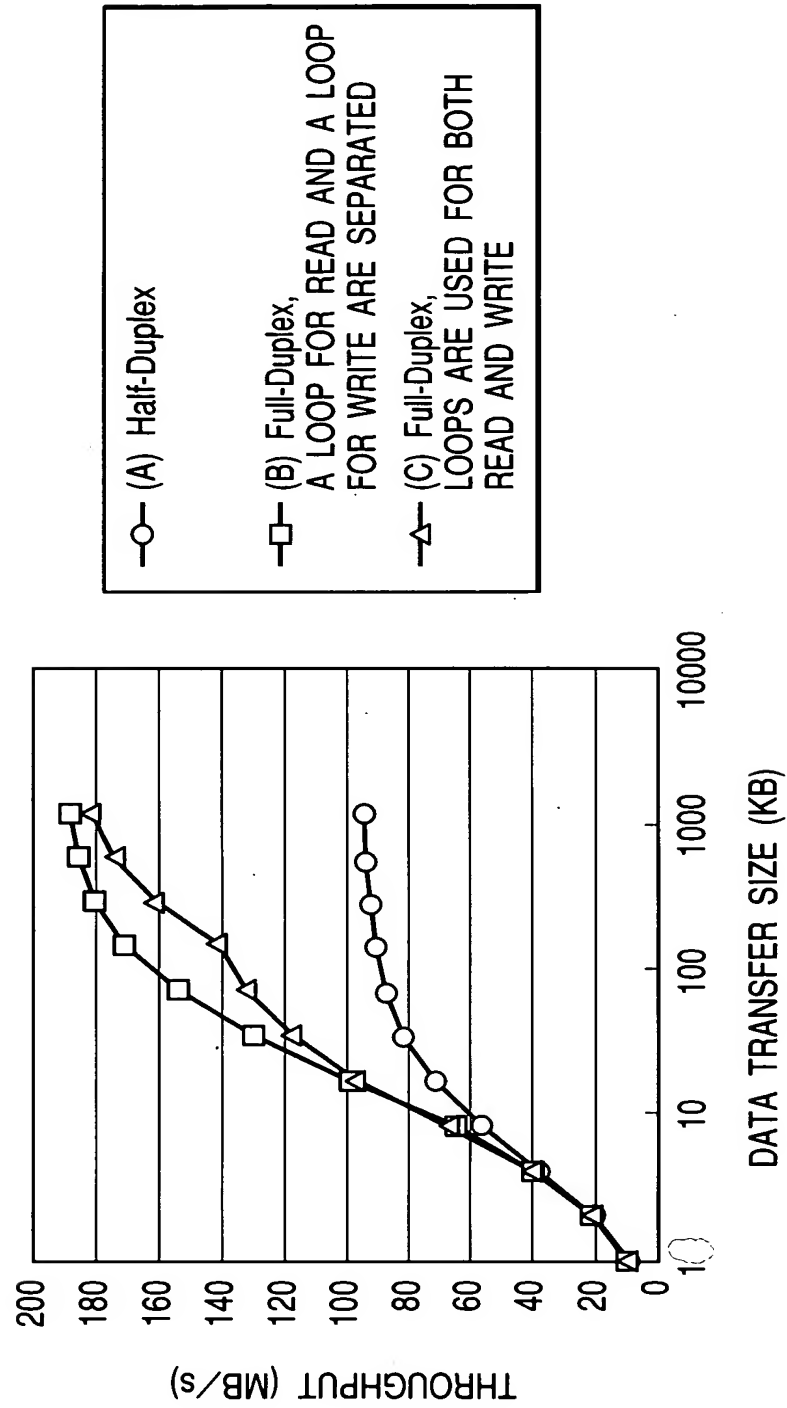
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FIG. 15



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FIG. 16

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DRIVE NO.	VDEV	WITHOUT FAILURE			WHEN SW1 FAILS		WHEN SW2 FAILS	
		DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R/W Drive Port
0	0	0	PID_0. a	PID_0. b	1	PID_0. b	0	PID_0. a
1			PID_1. a	PID_1. b		PID_1. b		PID_1. a
2			PID_2. a	PID_2. b		PID_2. b		PID_2. a
3			PID_3. a	PID_3. b		PID_3. b		PID_3. a
4	1	1	PID_4. a	PID_4. b	1	PID_4. b	0	PID_4. a
5			PID_5. a	PID_5. b		PID_5. b		PID_5. a
6			PID_6. a	PID_6. b		PID_6. b		PID_6. a
7			PID_7. a	PID_7. b		PID_7. b		PID_7. a
8	2	0	PID_8. a	PID_8. b	1	PID_8. b	0	PID_8. a
9			PID_9. a	PID_9. b		PID_9. b		PID_9. a
10			PID_10. a	PID_10. b		PID_10. b		PID_10. a
11			PID_11. a	PID_11. b		PID_11. b		PID_11. a
12	3	1	PID_12. a	PID_12. b	1	PID_12. b	0	PID_12. a
13			PID_13. a	PID_13. b		PID_13. b		PID_13. a
14			PID_14. a	PID_14. b		PID_14. b		PID_14. a
15			PID_15. a	PID_15. b		PID_15. b		PID_15. a

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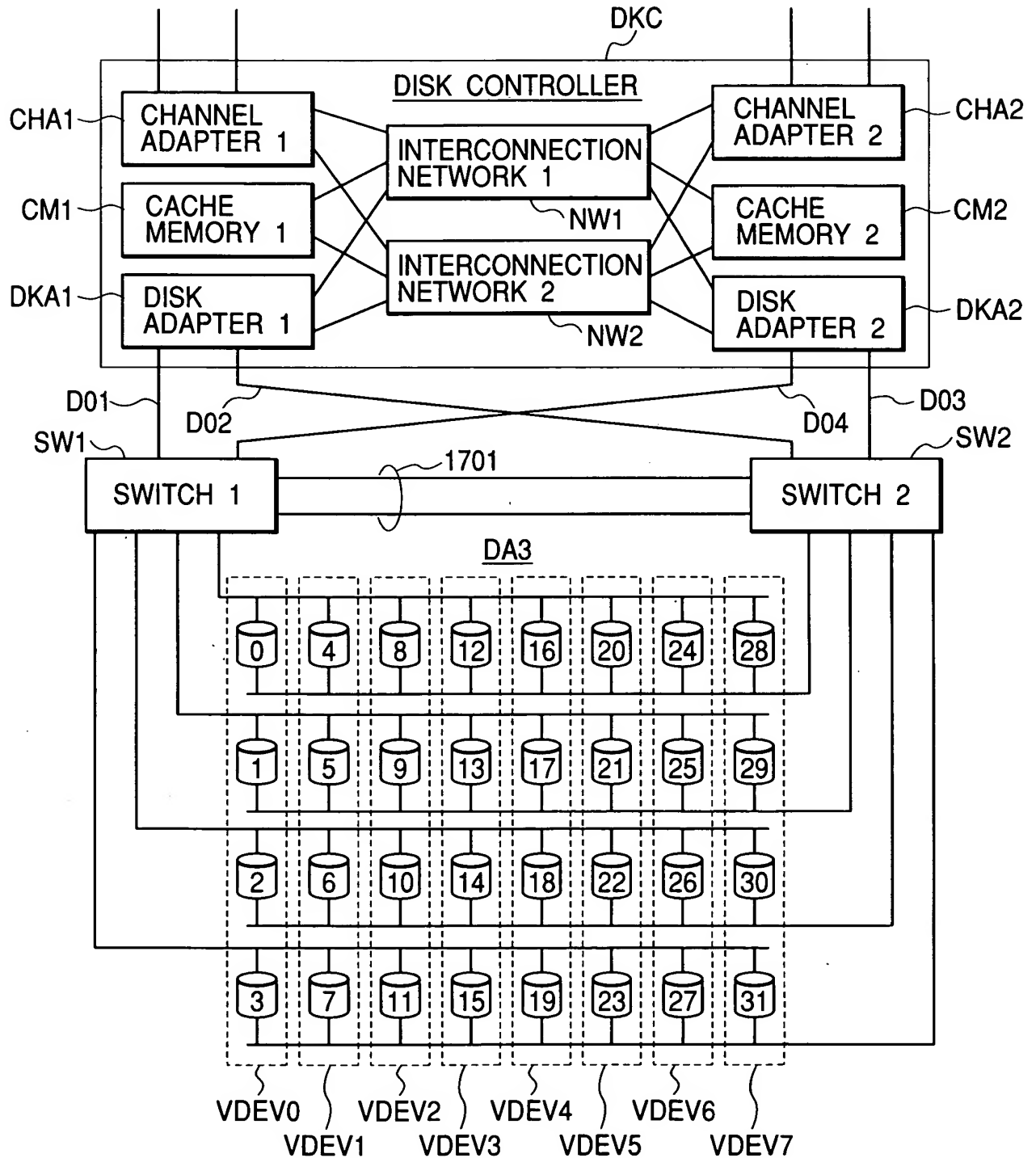
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FIG. 17



[illegible]

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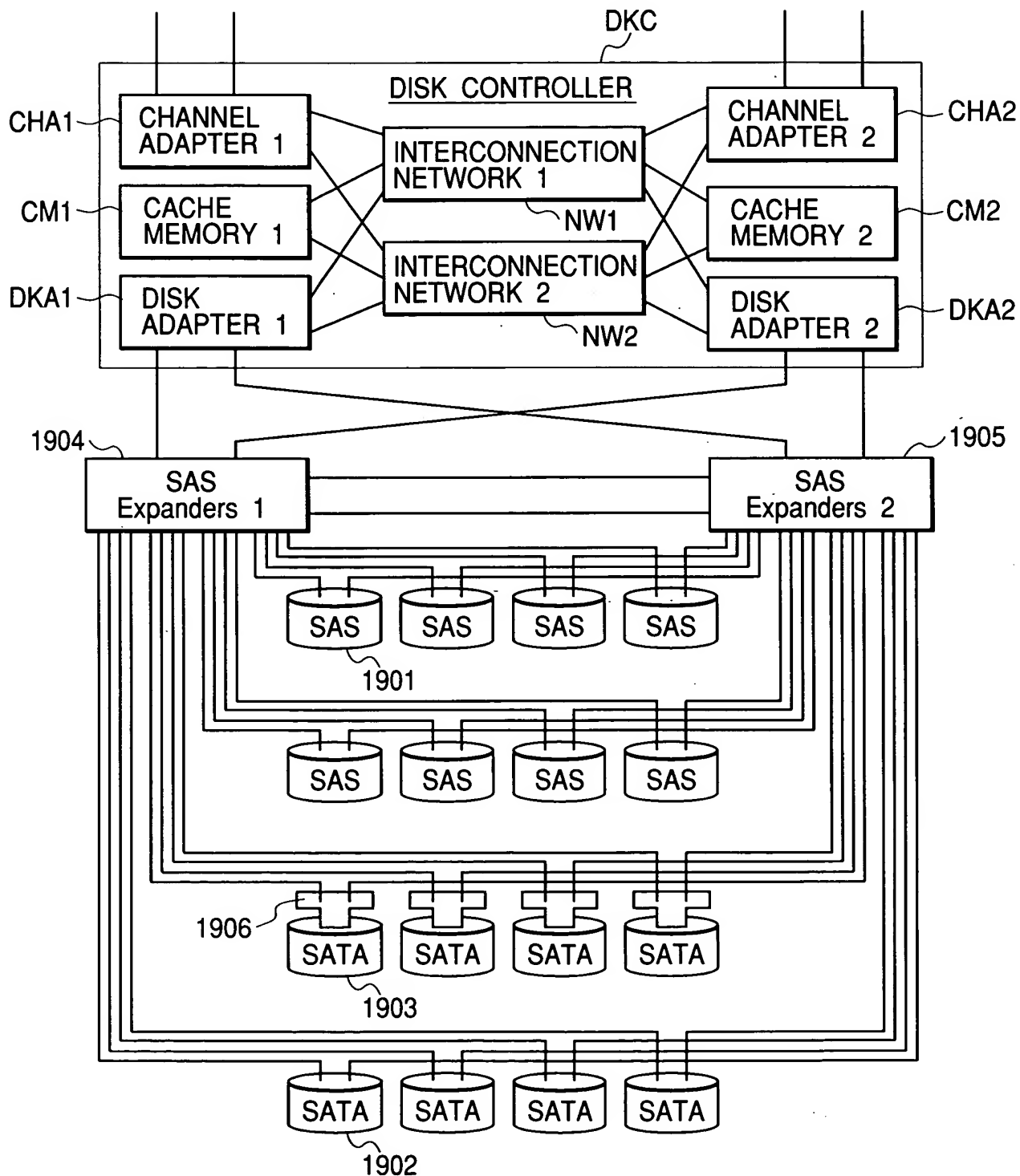
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FIG. 19



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FIG. 20

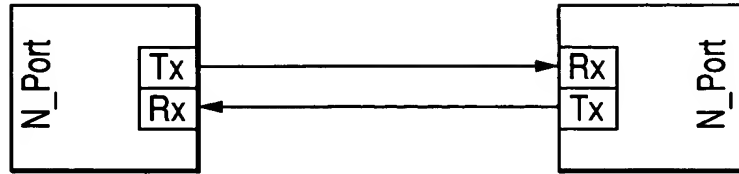


FIG. 21

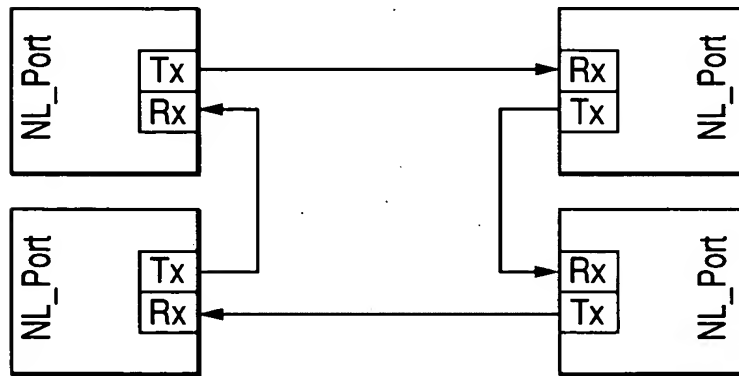
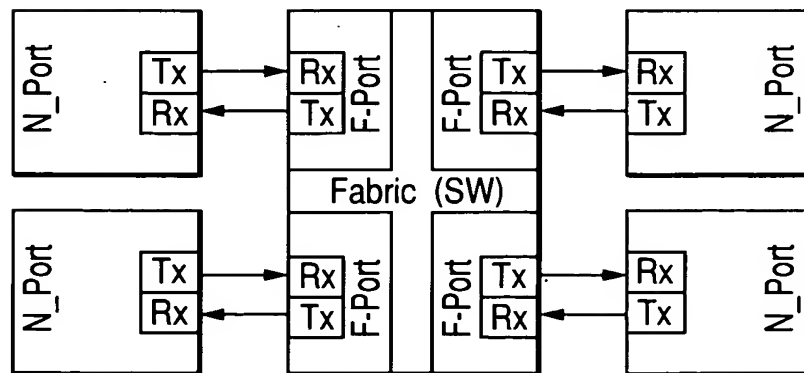


FIG. 22



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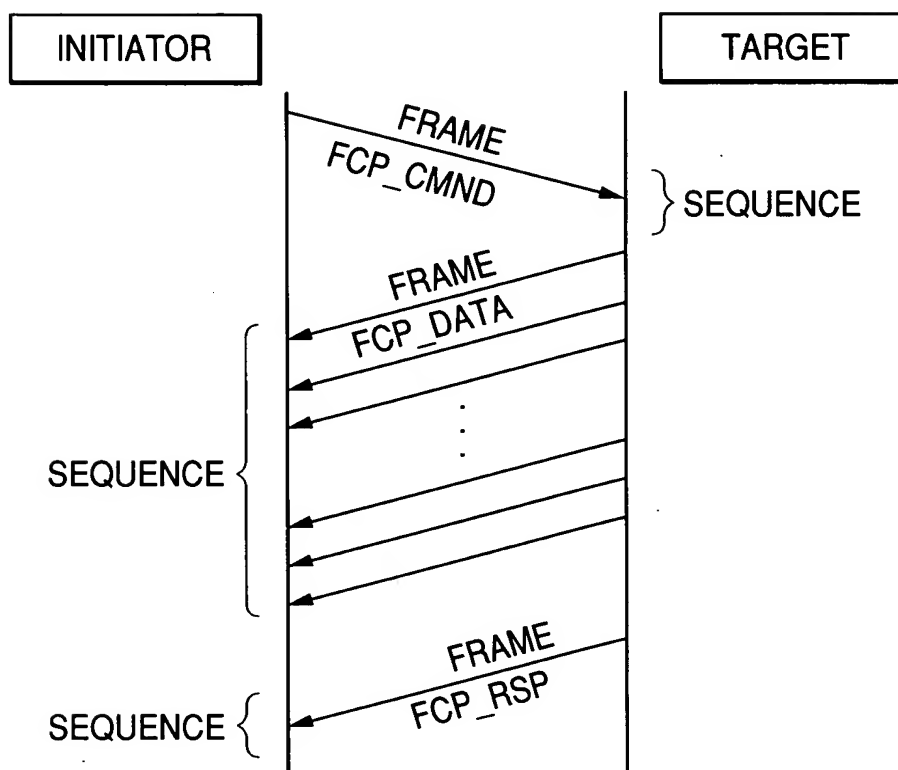
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FIG. 23



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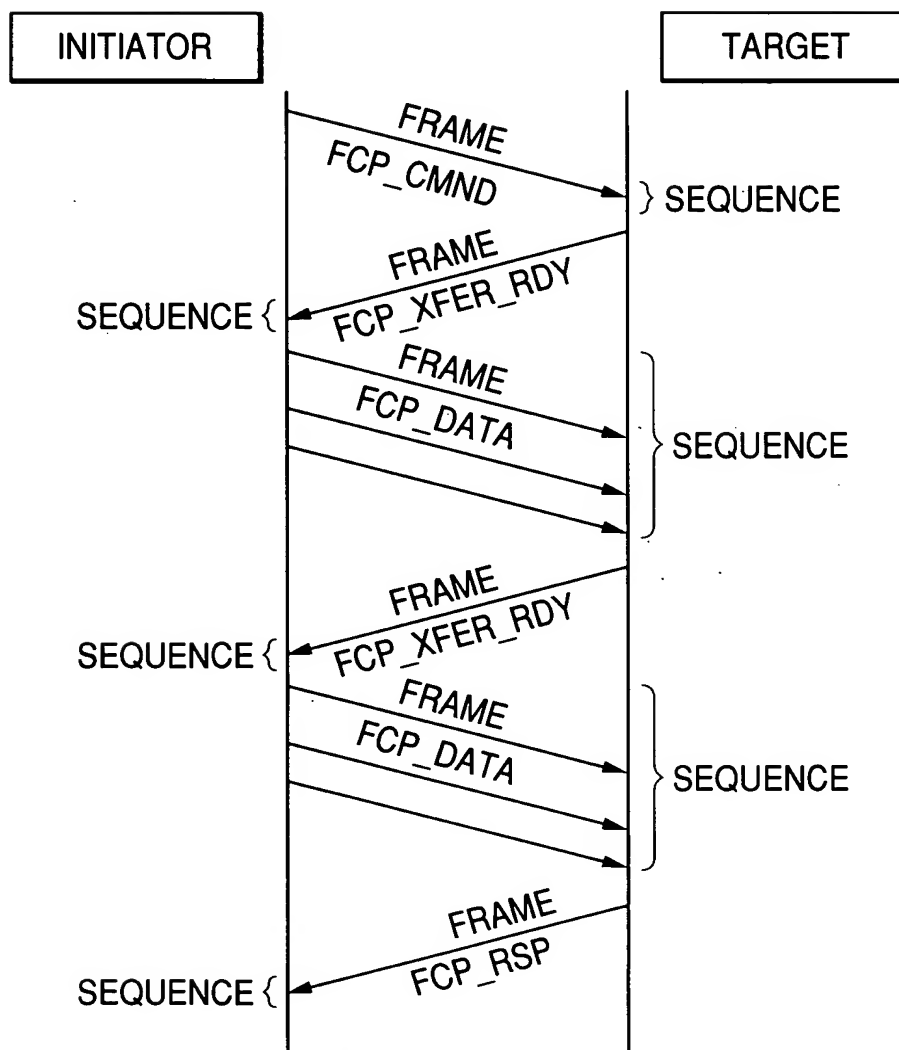
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FIG. 24



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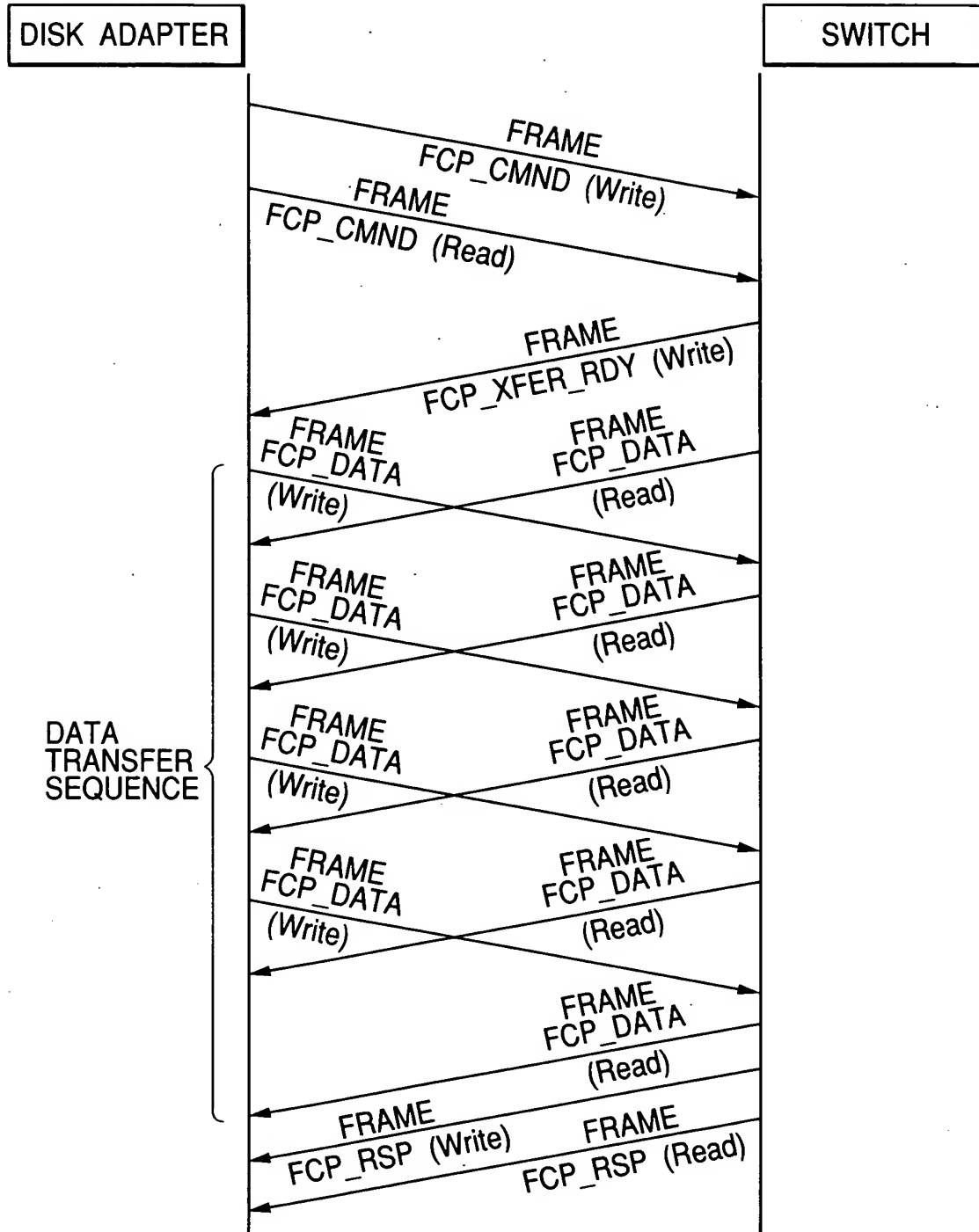
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FIG. 25



[illegible]